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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 08/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/798,751	PHAM, GIAO MINH	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the amendment filed 06/05/06. A new ground of rejection is introduced as necessitated by amendment. The allowable subject matters of claims 13 and 14 have been withdrawn.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Prater (USP 4829199).

As to claim 1, Prater's figure 6 shows a circuit, comprising: a first current limiting circuit (circuit 16 and the upper cascade states) including a first switch *(PMOS transistor, not shown, in circuit 29 that directly connected to the output terminal. It is noted that circuit 29 is an OR gate, and it is inherent that OR gate has PMOS and NMOS transistors)* and a first current source *(PMOS transistors on the right of 27 and 16 respectively)* coupled between a selector terminal (output) and a first voltage bus (Vdd), wherein the selector terminal is coupled to select a mode of operation of an integrated circuit *(circuit, not shown, that receives the output signal)*, the first current limiting having a first fixed current limit value *(current value of the PMOS transistor on the right of 16)* and a third fixed current limit value *(current values of both PMOS transistors on the right of 16 and 27)*, the first current limiting circuit adapted to limit a current out of the selector terminal to the first fixed current limit value or the third fixed current limit value in response to a voltage on the selector terminal; and a second current limiting circuit *(circuit 18 and the lower cascade states)* including a second switch *(NMOS transistor in 31 that directly*

connected to the output terminal. It is noted that circuit 31 is an AND gate. It is inherent that AND gate has PMOS and NMOS transistors) and a second current source (N*MOS transistors in the right of 18, 28 and 31 respectively)* coupled between the selector terminal and a second voltage bus (ground), the second current limiting circuit having a second fixed current limit value *(current value of both NMOS transistors on the right of 18 and 28)* and a fourth fixed current limit value (values of NMOS transistors on the right of 18, 28 and 31), the second current limiting circuit adapted to limit a current limit into the selector terminal to the second fixed current limit value or fourth fixed current limit value in response to the voltage on the selector terminal.

As to claim 2, figure 6 shows a plurality of voltage comparators (27 and 28) coupled to the selector terminal.

As to claim 3, figure 6 shows a decoder circuit (29, 31) coupled to the plurality of voltage comparators.

As to claim 4, figure 6 shows the first current limiting circuit includes a first variable current source comprising the first current source (PMOS transistor in the right of 16) and a third current source (PMOS transistor on the right of 27) coupled between the first voltage bus the selector terminal.

As to claim 5, figure 6 shows that the first switch (the PMOS, not shown, in 29) is adapted to conduct when the voltage on the selector terminal is below a first threshold voltage (voltage level that low enough to turn on the PMOS), the first switch is adapted not to conduct when the voltage on the selector terminal is above a second threshold voltage (voltage level that is high enough to turn off the PMOS).

As to claim 6, figure 6 shows that the second current limiting circuit includes a second variable current source comprising the second current source (NMOS transistors on the right of 18 and 28) and a fourth current source (NMOS on the right of 31).

As to claim 7, figure 6 shows that the second switch (the NMOS, not shown, in 31) is adapted to conduct when the voltage on the selector terminal is above a third threshold voltage, the second switch is adapted not to conduct when the voltage on the selector terminal is below a fourth threshold voltage.

As to claim 8, figure 6 shows that the first current limiting circuit is adapted to limit the current out of the selector terminal to the first fixed current limit value when the voltage on the selector terminal is below a fifth threshold voltage (fifth threshold voltage may be any value), the first current limiting circuit is adapted to limit the current out of the selector terminal to a third fixed current limit value when the voltage on the selector terminal is above a sixth threshold voltage (sixth threshold voltage may be any value).

As to claim 9, figure 6 shows that the second current limiting circuit is adapted to limit the current into the selector terminal to the second fixed current limit value when the voltage on the selector terminal is above a seventh threshold voltage (seventh threshold may be any value), wherein the second current limiting circuit is adapted to limit the current into the selector terminal to the fourth current limit when the voltage on the selector terminal is below an eighth threshold voltage (eighth threshold voltage may be any value).

As to claim 10, it is inherent that the first and second threshold voltages are less than the third and fourth voltages.

As to claim 11, figure 6 shows the fifth threshold voltage and the sixth threshold voltage are lower than the first threshold voltage and the second threshold voltage (as noted above, the fifth and sixth threshold voltages may be any values).

As to claim 12, figure 6 shows that the seventh threshold voltage and the eighth threshold voltage are higher than the third threshold voltage and the fourth threshold voltage (as noted above, the seventh and eight threshold voltages may be any values).

As to claim 13, figure 6 shows that the first fixed current limit is less than the second fixed current limit.

As to claim 14, figure 6 shows that the third fixed current limit is less than the fourth fixed current limit.

As to claim 15, figure 6 shows that the circuit further included in an integrated circuit.

As to claim 16, figure 6 shows that the integrated circuit device is a controller in a switching power supply.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

QUAN TRA
PRIMARY EXAMINER
ART UNIT 2816

July 26, 2006